Improved Read Voltage Margins with Alternative Topologies for Memristor-based Crossbar Memories

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Abstract—Memories based on hysteretic resistive materials are expected to have superior properties such as nonvolatility, low power consumption, as well as very high capacity. Crossbar arrays are considered very attractive for future ultimately scaled memories. In this paper, the memristor-based passive crossbar geometry is studied and a set of different topological patterns, which introduce insulating junctions within the memory array, is presented. In the worst-case reading scenario the simulations revealed significantly improved sensed voltage margins (up to > 4×) which alleviate the rigorous requirement for large and high-performance CMOS sensing circuits in passive crossbar memory systems.

Keywords—memristor; crossbar; memory; nano-scale circuits; resistive random access memory

I. INTRODUCTION

Nowadays, nonvolatile resistive random access memory (ReRAM) [1-2] is considered as a promising alternative to conventional flash-based memory due to the prospect of high scalability and low power consumption. Related work in nano-scale memory design has predominantly focused on crossbar-based architectures. The crossbar geometry [3] consists of two sets of parallel wires crossing perpendicularly, with the region where two wires cross being a junction which may either be configured as an electronic device (e.g. a bistable memory device) or left unconfigured, so that the two crossing wires do not interact electrically. Crossbars offer several benefits including a regular pattern, compatibility with CMOS processes, large connectivity and the highest possible device density [4]. Passive nano-crossbar arrays comprising bipolar switchable resistors have been proposed as convenient geometries in order to achieve higher density and performance in nonvolatile ReRAMs [5]. Hereinafter we will simply refer to the aforementioned resistors as memristors, based on the recent discovery by HP [6] of the first modern example of this fundamental circuit component. In a typical passive crossbar memory, where no rectifying devices are used to isolate the cells being written or read [7], the existence of parasitic conducting (current sneak-paths) reduces the maximum achievable size of the crossbar array that still allows a reliable distinction between the two possible conducting states of a junction. This qualifies the implementation of high-performance CMOS read and write circuits to a key element for the success of large purely passive crossbar arrays.

In the present work a memristive passive crossbar memory system is studied. A set of different topological array patterns which incorporate insulating junctions are introduced in order to investigate their effect on the read-out sense voltage margins for array sizes with up to 4096 elements. The crossbar is accessed following the approach of reading one bit at a time and the worst case reading scenario is examined. The reported simulation results show that the worst-case sensed voltage margin in a specific crossbar size can be significantly increased (up to > 4×) by introducing a certain percentage of insulating nodes. Such an approach may prove advantageous in terms of simplified fabrication processes of large memory arrays by alleviating the requirement for large and high-performance CMOS sensing circuits.

II. SETUP OF MEMRISTOR-BASED CROSSBAR MEMORY

In this work, the study of a nano-scale crossbar memory system that uses memristors with highly nonlinear current–voltage characteristics as memory elements is discussed. Such a system does not utilize the kind of devices (diodes or transistors) that are normally used to isolate the cell being written to and read from in conventional memories. The simplest circuit approach for reading information from the memristor-based crossbar is by applying a certain read voltage across a junction and transforming the current flow into a voltage. Column and row decoders drive the necessary selection switches in order to form a voltage divider circuit with the corresponding pull-up resistor and the resistance of the accessed node. The output of the voltage divider is then driven to a CMOS sense amplifier and the state of the device is distinguished by comparing this voltage to a reference value. The voltage swing at the output of the crossbar read circuit between reading a high impedance state (R_OFF) and a low impedance state (R_ON) should be large enough for the two states to be easily distinguishable. The equivalent circuits of a
read operation in a passive crossbar are given in Fig. 1. In the ideal reading case, where no current sneak paths are present, the equivalent circuit for the read operation is a simple voltage divider formed by a pull-up resistor \( R_{\text{PU}} \) and the accessed memristor (Fig. 1b). For a given \( R_{\text{OFF}}/R_{\text{ON}} \) ratio the achieved voltage swing \( \Delta V \) for a certain applied pull-up voltage \( V_{\text{PU}} \) is calculated as follows:

\[
\Delta V = \frac{V_{\text{OFF}} - V_{\text{ON}}}{V_{\text{PU}}} = \frac{R_{\text{OFF}}}{R_{\text{OFF}} + R_{\text{PU}}} - \frac{R_{\text{ON}}}{R_{\text{ON}} + R_{\text{PU}}}
\]  

(1)

This normalized detection margin of the two possible states of a memory cell is maximized if the pull-up resistor \( R_{\text{PU}} \) is optimally chosen; for large \( R_{\text{OFF}}/R_{\text{ON}} \) ratios optimal \( R_{\text{PU}} \) is close to \( R_{\text{ON}} \). Unfortunately in real reading operation, with parasitic current paths in parallel to the accessed memristor, the effective \( R_{\text{OFF}}/R_{\text{ON}} \) ratio results substantially smaller (Fig. 1c). The impact of parasitic sneak paths definitely depends on the way the crossbar is accessed. Here a crossbar-setup with \( m \) wordlines and \( n \) bitlines is assumed, where the resistance of the selection transistors and interconnects is neglected. Among different approaches of accessing the crossbar, one is to select one wordline, pull up one bitline and leave the other bitlines floating, thus the reading operation assumes accessing one bit at a time. The worst case scenario for reading the crossbar is the following: when reading a memristor found in the OFF state and the parasitic resistance is as small as possible, the crossbar output voltage notably degrades. This is the case where all non-accessed memristors are set to ON, i.e. \( R_{\text{sneak}} = R_{\text{ON}} \) (see Fig. 1). The corresponding worst case scenario for reading a memristor found in the ON state assumes that all non-accessed nodes are set to the OFF state [1-2]. The parasitic worst case resistance for an \( n\times m \)-crossbar can be computed using the equivalent circuit shown in Fig. 1c.

The maximum achievable read voltage margin gets significantly smaller with increasing crossbar size, regardless of the chosen resistance ratio [2] and even with the sense resistance value for each array chosen with its optimum value to maximize the detection margin [1]. It is therefore evident that innovative techniques which will enlarge significantly the measured voltage margins, constitute a key factor towards the practical realization of passive crossbar memory systems.

III. ALTERNATIVE CROSSBAR TOPOLOGY PATTERNS

In this section, a set of special topology patterns for passive crossbar memories is introduced. Such alternative topologies comprise a certain percentage of insulating nodes spread out inside the array according to specific distribution patterns. The motivation is to restrain current sneak-paths and thus improve the voltage margins by replacing some memory cells. Such a practice is considered a viable solution given the huge device density that the crossbar geometry offers compared to other circuit architectures. A summary of the tested patterns is depicted in Fig. 2 where red dots denote insulating nodes and simple wire crossings denote memristors. All patterns are tested both for \( 32\times32 \) and \( 64\times64 \) grid sizes in the worst case reading scenario. As far as the amount of the inserted insulators is concerned, three different cases are examined where their number approximates 10%, 25% or 50% of the total nodes of the grid under consideration. In each case the selected distribution of the insulating junctions aims to uniformly cover the entire area of the grid, as much as this is possible, depending on the specific pattern and the actual grid size. These topologies are described in details as follows:

In the “Columns” pattern the insulating junctions are located in columns that are uniformly distributed across the array. In the “Rows” pattern the same details apply, only that the insulating junctions are now placed in rows. The “Columns and Rows” pattern turns up if the two previously mentioned patterns are superimposed. In this case the resulting total number of inserted insulators is greater and approximates the percentages 17%, 43% and 75%, respectively. In the “Rectangular Rings” pattern the inserted insulating nodes are
placed in rectangular rings formations which are distributed across the grid starting from the central four nodes, i.e. the innermost ring. Finally, in the “Uniformly Distributed” pattern, the insulating nodes are placed in such a manner, in order to be uniformly distributed both horizontally and vertically inside the grid. For each insulator, the closest neighboring insulating nodes are always found at equal horizontal and vertical distances and the grid is considered a ‘torus’ to facilitate the distribution. At this point, an easy conclusion would be that, the greater the percentage of the inserted insulating nodes, the higher the read-out voltages will be measured, given that the remaining memristors are less and thus the total memory is smaller. However, we next prove that replacing certain percentage of memory cells with insulating nodes does not deliver the same voltage margins with a smaller memory, i.e. a memory whose number of memristors equals the number of the remaining memristors if we omit the insulators.

IV. WORST-CASE MEASUREMENT SIMULATIONS

Simulations are based on a device model for memristors derived from [8]. Nodal analysis is performed and all differential equations are numerically solved using a 4th order Runge-Kutta integration method. It is assumed that all memristors are identical with resistance ratio \( R_{OFF}/R_{ON} = 200 \) and the sense resistor \( R_{SL} \) is set to the optimum value to yield the highest possible signal to noise ratio for the output voltages. The resistances of interconnects are not considered here, but it has been shown that they further degrade voltages when approaching the middle of the crossbar field [1].

The presented patterns are tested for both 32×32 and 64×64 grids and their performance is compared to that of the full memristive crossbar. Three different distribution categories are considered, characterizing the total population of insulators in the grid which each time approximates 10%, 25% or 50% of the total number of nodes. The worst-case reading scenario is performed by applying a 1V read pulse across the target cell and thus calculating the resulting voltage margin. The summary of the patterns’ performance for the two grid sizes is shown in Fig. 3. In each graph the voltage margins (\( \Delta V/V_{PU} \)) are normalized to the reference value which is always the performance of the full memristive crossbar. However, as a figure of merit, the measured voltage margins of smaller arrays are also included in each graph. The actual sizes of these arrays (in number of memory cells) result if we remove the insulating junctions from the grids and keep the remaining memristors. For example in Figs. 3a, 3d, apart from the full crossbar (32×32 and 64×64), smaller grids which incorporate 90% of the cells of the reference grids (i.e. 100% minus the distribution percentage) are also examined. It can be seen that for all tested patterns the measured voltage margins are improved but they are never equal to the values which correspond to the smaller memristive grids.

More specifically, Fig. 3a shows that by moving from a 32×32 grid to a smaller configuration with 10% less nodes, the voltage margins increase by 14%. However, by maintaining the same grid size but replacing 10% of the nodes with insulators, the observed changes at the voltage margins range between 1% and 31% depending on the selected topology. Likewise, in Fig. 3b a grid with 25% less nodes results in 31% improved voltage margin whereas introducing 25% insulators delivers improvement ranging between 3% and 81%. Finally, Fig. 3c indicates that a grid with half of the initial nodes almost doubles the measured voltage margins whereas the presented patterns deliver up to 4× better read-out voltages. In Figs. 3d-f the same tests and the same proposed topological patterns apply to the 64×64 grid and similar results are extracted. As far as the overall patterns’ performance is concerned, both “Columns” and “Rows” result in the same improvements for all tested distribution scenarios. Their corresponding overlapping, i.e. “Columns and Rows”, returns significant changes but it is not considered as an attractive solution given that it calls for the introduction of almost twice as many insulating nodes as each one of the two separate patterns. “Rectangular Rings” pattern does not seem competitive for this type of reading approach. Moreover, in both of the simulated grid sizes, the “Uniformly Distributed” pattern restrains better the current sneak-paths and has the best performance in all of the simulation scenarios. Finally, it is worth noticing that in both grid sizes, application of the corresponding patterns delivers almost equal improvements,
even though the larger one of the tested grids comprises $4 \times$ more nodes, which means that such important improvement of the measured voltages is kept when moving to much larger quadratic memory crossbar arrays. The voltage improvement is also expected to be uniform in the crossbar field, even when considering the interconnection resistances with the measured DC voltages being degraded when approaching the middle of the crossbar array. The addressing scheme will be different to that of conventional memory arrays given that memory words include insulating elements.

V. CONCLUSIONS

This work introduces a set of alternative topologies for passive memristor-based crossbar memory systems which deliver significantly improved read-out voltages. The demonstrations in this paper verify that passive crossbar arrays, which do not require additional rectifying devices or special reading techniques, can indeed be built by employing the proposed alternative patterns. Therefore, this approach simplifies the array fabrication processes and alleviates the strict prerequisite for high-performance CMOS sensing circuits. Development of appropriate interface circuits for the aforementioned patterns will be part of our future work.

REFERENCES